<u>REMARKS</u>

Claims 4-6 and 24-26 have been amended herein to correct the spelling of the word "multiplexers."

Replacement Figures 1A-1F, 2, and 3 are attached hereto designated by the legend "Prior Art."

Claims 1-39 have been variously rejected based on the Tavana et al. reference (U.S. Patent No. 5,825,202.

In support of the rejection of claim 1, the examiner erroneously states that the Tavana et al. reference discloses "[sic] masked programmed dedicated interface tracks connected logic blocks in the FPGA and mask programmed interconnect conductors in the ASIC portion: Tavana discloses mask-defined routing for interconnecting FPGA and ASLA (FIG. 3, #20, #18)." In fact, Tavana et al. disclose no such thing.

Further, with respect to the rejection of claim 21, the examiner asserts that Tavana et al. disclose "mask programmed interconnect tracks connectde [sic] logic blocks in the FPGA and mask programmed interconnect conductors in the ASIC portion: Tavana discloses mask-defined routing for interconnecting FPGA and ASLA (FIG. 3, #18, #20)." Here too, Tavana et al. disclose no such thing.

This feature of the present invention as claimed in claims 1 and 21 is not disclosed or suggested at all by the Tavana et al. reference. As plainly shown in the reference at FIG. 3 relied upon by the examiner, Tavana et al. disclose that The mask-defined routing 18 connects only the ASLA 14 to the programmable routing 20. The programmable routing 20 must further be programmed to connect elements in the ASLA 14 to any element in a CLB through programmable routing 20 and further through switch matrix routing in the FPGA.

According to the Tavana et al. reference, the programmable routing 20 is not even part of the FPGA. As disclosed in the reference [col. 5, lines 13-15 (emphasis added)]: "As shown further in FIG. 2, the arrays 12 and 14 *are surrounded by* two distinct forms of routing, namely mask-defined routing 18 and programmable routing 20." Thus, Tavana et al. do not consider the programmable routing 20 to be part of the FPGA. Clearly, and as shown in FIG. 3, the only routing associated with the FPGA are the blocks labeled "switch matrix" that are, in turn, *programmably* connected to the programmable routing 20.

The claim language at issue here is "mask programmed dedicated interface tracks connected between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion" in claim 1 and "mask programmed dedicated interface tracks connected between said modules or blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion" in claim 21. This feature of the claimed invention is not disclosed or suggested in the Tavana et al. reference, since programmable connections MUST be made in BOTH programmable routing 20 (which is not part of the FPGA) and in at least one programmable "switch matrix" in the FPGA before a connection can be completed to a CLB (which is the equivalent of one of the "logic blocks" as recited in claim 1, or "modules or blocks" as recited in claim 21). At best, the Tavana et al. reference shows mask programmable dedicated interconnect conductors connected between the ASLA and the programmable routing 20 which, as clearly shown in FIG. 3 of the reference, is not the FPGA portion of the device and certainly is not a logic block or module within the FPGA portion.

Accordingly, the Tavana et al. reference does not disclose or suggest the limitations of claims 1 and 21 "mask programmed dedicated interface tracks connected between said logic blocks in said FPGA portion and said mask programmed interconnect

conductors in said ASIC portion" in claim 1 and "mask programmed dedicated interface tracks connected between said modules or blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion" in claim 21. These limitations require that the mask-programmable conductors make connections between the ASIC portion and the individual logic blocks in the FPGA portion. If the Examiner thinks that the Tavana et al. reference discloses mask-programmable conductors that connect the ASIC portion of the disclosed device to individual logic modules in the disclosed device the undersigned respectfully requests that the Examiner point out the specific places in the reference containing such disclosure.

Because of this failure, the Tavana et al. reference cannot be used to reject independent claims 1 and 21, which are thus patentable over this reference. Since the remaining claims in the application depend from either claim 1 or claim 21, they are likewise patentable over the reference.

If the Examiner has any questions regarding this application or this response, the Examiner is requested to telephone the undersigned at 775-586-9500.

Respectfully submitted,
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